CLAIMS

1. An integrated circuit active memory device fabricated on a single semiconductor substrate, the active memory device comprising:

a memory device having a data bus containing a plurality of data bus bits;

an array of processing elements with each processing element coupled to a respective group of the data bus bits, each of the processing elements having an instruction input coupled to receive processing element instructions for controlling the operation of the processing elements;

an array control unit coupled to the processing elements in the array, the array control unit being operable to generate and to couple respective sets of the processing element instructions to the processing elements responsive to each of a plurality of array control unit commands applied to a command input of the array control unit;

a memory device control unit coupled to the memory device, the memory device control unit being operable to generate and to couple respective sets of memory commands to the memory device responsive to each of a plurality of memory device control unit commands applied to a command input of the memory device control unit; and

a command engine coupled to the array control unit and the memory device control unit, the command engine being operable to couple to the array control unit respective sets of the array control unit commands and to couple to the memory device control unit respective sets of the memory device control unit commands responsive to respective task commands applied to a task command input of the command engine.

2. The active memory device of claim 1 wherein the memory device comprises a dynamic random access memory device.

3. The active memory device of claim 1, further comprising a memory device interface having a first set of terminals that are externally accessible from outside the integrated circuit and a second set of terminals that are coupled to the memory device, the memory device interface being operable to allow data to be externally written to and read from the memory device without being coupled through the memory device control unit.

4. The active memory device of claim 1, further comprising an array control unit bypass path allowing the command input of the array control unit to be coupled directly to the task command input.

5. The active memory device of claim 1, further comprising a memory device control unit bypass path allowing the command input of the memory device control unit to be coupled directly to the task command input.

6. The active memory device of claim 1 wherein the array control unit is operable to store the processing element instructions at respective addresses in a storage device included in the array control unit, and wherein the array control unit commands generated by the command generator comprise respective storage device addresses.

7. The active memory device of claim 1 wherein the array control unit commands are at a higher level than the respective task commands.

8. The active memory device of claim 1 wherein the memory device control unit commands are at a higher level than the respective task commands.

9. The active memory device of claim 1 wherein each of the task commands comprise:

at least one device select bit that designates the task command as either a task command for the processing elements or a task command for the memory device, and

a plurality of command data bits.

10. The active memory device of claim 9 wherein each of the task commands further comprise a plurality of device specific function bits that designate the function to be performed by the processing elements if the device select bit designates the processing elements and the function to be performed by the memory device if the device select bit designates the memory device.

11. The active memory device of claim 1 wherein the command engine comprises an internal instruction cache storing a plurality of instructions at respective addresses, and wherein the instruction cache is programmable to allow sets of instructions to be stored in the cache based on the nature of the task commands that will be applied to the task command input of the command engine.

12. The active memory device of claim 11 wherein the command engine comprises a program counter coupled to the instruction cache, the program counter outputting a program count that is used as the address for the instruction cache.

13. The active memory device of claim 12 wherein one of the task commands comprises a jump command including a jump address, and wherein the

command engine is operable to preset the program counter to a count corresponding to the jump address responsive to decoding the jump command.

14. The active memory device of claim 12 wherein the command engine further comprises an adder coupled to the program counter to offset the count of the program counter by a predetermined magnitude.

15. The active memory device of claim 11 wherein the command engine further comprises a register file coupled to the instruction cache, the register file being operable to store data at locations corresponding to respective addresses, the register filed being addressed by at least a portion of the instructions stored in the instruction cache.

16. The active memory device of claim 1 wherein the command engine further comprises:

an arithmetic and logic unit; and

a register coupled to receive and store data resulting from an arithmetic or logical operation performed by the arithmetic and logic unit, the register applying the stored data to the array control unit and to the memory device control unit.

17. The active memory device of claim 16 wherein the arithmetic and logic unit is operable to receive data stored in the register responsive to a previous an arithmetic or logical operation.

18. The active memory device of claim 1 wherein the command engine further comprises at least one defer buffer operable to store the memory device control unit commands and to subsequently couple the memory device control unit commands to the memory device control unit.

19. An active memory control system, comprising:

a first control device receiving task commands corresponding to respective active memory operations, the first control device being operable to generate either a respective set of memory commands or a respective set of processing commands responsive to each of the task commands;

a second control device coupled to receive the memory commands from the first control device, the second control device being operable to generate a respective set of the memory device instructions responsive to each of the memory commands; and

a third control device coupled to receive the processing commands from the first control device, the third control device being operable to generate a respective set of the processing element instructions responsive to each of the processing commands.

20. The active memory control system of claim 19 wherein the processing commands are at a higher level than the respective task commands.

21. The active memory control system of claim 19 wherein each of the task commands comprise:

at least one device select bit that designates the task command as either a task command for the processing elements or a task command for the memory device, and

a plurality of command data bits.

22. The active memory control system of claim 21 wherein each of the task commands further comprise a plurality of device specific function bits that designate the function to be performed by the processing elements if the device select

bit designates the processing elements and the function to be performed by the memory device if the device select bit designates the memory device.

23. The active memory control system of claim 19 wherein the first control device comprises an instruction cache storing a plurality of instructions at respective addresses, and wherein the instruction cache is programmable to allow sets of instructions to be stored in the cache based on the nature of the task commands that are received by the first control device.

24. The active memory control system of claim 23 wherein the first control device comprises a program counter coupled to the instruction cache, the program counter outputting a program count that is used as the address for the instruction cache.

25. The active memory control system of claim 24 wherein one of the task commands comprises a jump command including a jump address, and wherein the first control device is operable to preset the program counter to a count corresponding to the jump address responsive to decoding the jump command.

26. The active memory control system of claim 24 wherein the first control device further comprises an adder coupled to the program counter to offset the count of the program counter by a predetermined magnitude.

27. The active memory control system of claim 23 wherein the first control device further comprises a register file coupled to the instruction cache, the register file being operable to store data at locations corresponding to respective addresses, the register filed being addressed by at least a portion of the instructions stored in the instruction cache.

28. The active memory control system of claim 19 wherein the first control device further comprises:

an arithmetic and logic unit; and

a register coupled to receive and store data resulting from an arithmetic or logical operation performed by the arithmetic and logic unit, the register applying the stored data to either the second control device or the third control device.

29. The active memory control system of claim 28 wherein the arithmetic and logic unit is operable to receive data stored in the register responsive to a previous an arithmetic or logical operation.

30. The active memory control system of claim 19 wherein the first control device further comprises at least one defer buffer operable to store the memory commands and to subsequently couple the memory commands to the second control device.

31. The active memory control system of claim 19 wherein the first control device, the second control device and the third control device are fabricated on a common integrated circuit substrate.

32. A computer system, comprising:

a host processor having a processor bus;

at least one input device coupled to the host processor through the processor bus;

at least one output device coupled to the host processor through the processor bus;

at least data storage device coupled to the host processor through the processor bus; and

an active memory device, comprising:

a memory device having a data bus containing a plurality of data bus bits;

an array of processing elements with each processing element coupled to a respective group of the data bus bits, each of the processing elements having an instruction input coupled to receive processing element instructions for controlling the operation of the processing elements;

an array control unit coupled to the processing elements in the array, the array control unit being operable to generate and to couple respective sets of the processing element instructions to the processing elements responsive to each of a plurality of array control unit commands applied to a command input of the array control unit;

a memory device control unit coupled to the memory device, the memory device control unit being operable to generate and to couple respective sets of memory commands to the memory device responsive to each of a plurality of memory device control unit commands applied to a command input of the memory device control unit; and

a command engine coupled to the array control unit and the memory device control unit, the command engine being operable to couple to the array control unit respective sets of the array control unit commands and to couple to the memory device control unit respective sets of the memory device control unit commands responsive to respective task commands applied to a task command input of the command engine from the host processor.

33. The computer system of claim 32 wherein the memory device comprises a dynamic random access memory device.

34. The computer system of claim 32, further comprising a memory device interface having a first set of terminals that are externally accessible from outside the integrated circuit and a second set of terminals that are coupled to the memory device, the memory device interface being operable to allow data to be externally written to and read from the memory device without being coupled through the memory device control unit.

35. The computer system of claim 32, further comprising an array control unit bypass path allowing the command input of the array control unit to be coupled directly to the task command input.

36. The computer system of claim 32, further comprising a memory device control unit bypass path allowing the command input of the memory device control unit to be coupled directly to the task command input.

37. The computer system of claim 32 wherein the array control unit is operable to store the processing element instructions at respective addresses in a storage device included in the array control unit, and wherein the array control unit commands generated by the command generator comprise respective storage device addresses.

38. The computer system of claim 32 wherein the array control unit commands are at a higher level than the respective task commands.

39. The computer system of claim 32 wherein the memory device control unit commands are at a higher level than the respective task commands.

40. The computer system of claim 32 wherein each of the task commands comprise:

at least one device select bit that designates the task command as either a task command for the processing elements or a task command for the memory device, and

a plurality of command data bits.

41. The computer system of claim 40 wherein each of the task commands further comprise a plurality of device specific function bits that designate the function to be performed by the processing elements if the device select bit designates the processing elements and the function to be performed by the memory device if the device select bit designates the memory device.

42. The computer system of claim 32 wherein the command engine comprises an internal instruction cache storing a plurality of instructions at respective addresses, and wherein the instruction cache is programmable to allow sets of instructions to be stored in the cache based on the nature of the task commands that will be applied to the task command input of the command engine.

43. The computer system of claim 42 wherein the command engine comprises a program counter coupled to the instruction cache, the program counter outputting a program count that is used as the address for the instruction cache.

44. The computer system of claim 43 wherein one of the task commands comprises a jump command including a jump address, and wherein the command engine is operable to preset the program counter to a count corresponding to the jump address responsive to decoding the jump command.

45. The computer system of claim 43 wherein the command engine further comprises an adder coupled to the program counter to offset the count of the program counter by a predetermined magnitude.

46. The computer system of claim 42 wherein the command engine further comprises a register file coupled to the instruction cache, the register file being operable to store data at locations corresponding to respective addresses, the register filed being addressed by at least a portion of the instructions stored in the instruction cache.

47. The computer system of claim 32 wherein the command engine further comprises:

an arithmetic and logic unit; and

a register coupled to receive and store data resulting from an arithmetic or logical operation performed by the arithmetic and logic unit, the register applying the stored data to the array control unit and to the memory device control unit.

48. The computer system of claim 16 wherein the arithmetic and logic unit is operable to receive data stored in the register responsive to a previous an arithmetic or logical operation.

49. The computer system of claim 32 wherein the command engine further comprises at least one defer buffer operable to store the memory device control unit commands and to subsequently couple the memory device control unit commands to the memory device control unit.

50. The computer system of claim 32 wherein the array control unit, the memory device control unit and the command engine are fabricated on a common integrated circuit substrate.

51. The computer system of claim 32 wherein the array control unit, the memory device control unit, the command engine, the memory device and the processing elements are fabricated on a common integrated circuit substrate.

52. A method of controlling the operation of a memory device and an array of processing elements that are coupled to the memory device, the method comprising:

receiving a task command corresponding to an active memory operation;

responsive to the task command, generating either a set of array commands or a set of memory device commands;

responsive to each of the array commands, generating a respective set of processing element instructions;

responsive to each of the memory device commands, generating a respective set of memory device instructions;

coupling the processing element instructions to the processing elements; and

coupling the memory device instructions to the memory device.

53. The method of claim 52 wherein the memory device comprises a dynamic random access memory device.

54. The method of claim 52, further comprising generating a set of processing element instructions directly from a task command without first generating an array command.

55. The method of claim 52, further comprising generating a set of memory device instructions directly from a task command without first generating a memory device command.

56. The method of claim 42 wherein at least some of the array commands comprise respective storage device addresses, and wherein the act of generating the processing element instructions comprises:

storing the processing element instructions at respective addresses in a storage device; and

using the array commands to address the storage device.

57. The method of claim 42 wherein the task commands are at a higher level than the array commands in the respective set.

58. The method of claim 42 wherein the task commands are at a higher level than the memory device commands in the respective set.

59. The method of claim 42 wherein each of the task commands comprise:

at least one device select bit that designates the task command as either a task command for the processing elements or a task command for the memory device, and

a plurality of command data bits.

60. The method of claim 59 wherein each of the task commands further comprise a plurality of device specific function bits that designate the function to be performed by the processing elements if the device select bit designates the

processing elements and the function to be performed by the memory device if the device select bit designates the memory device.

61. The method of claim 42 wherein the act of generating the array commands and the memory device commands comprises:

storing a plurality of instructions in an instruction cache, the instructions being stored in the instruction cache based on the nature of the task commands from which the array command and the memory device commands will be generated;

using the task commands to address the instruction cache; and

generating the array commands and the memory device commands from the instructions stored in the instruction cache that are addressed by the task commands.

62. The method of claim 61 wherein the act of using the task commands to address the instruction cache comprises:

using a program counter to address the instruction cache; and

presetting the program counter to a count corresponding to a jump address in a jump task command.

63. The method of claim 62, further comprising offsetting the count of the program counter by a predetermined magnitude.

64. The method of claim 52 wherein the act of generating the memory device commands comprises deferring at least some of the memory device commands in a set from being generated responsive to a respective task command.

65. The method of claim 52 wherein the act of generating the array commands comprises deferring at least some of the array commands in a set from being generated responsive to a respective task command.